

Customer No.: 31561
Docket No.: 12386-US-PA
Application No.: 10/707,865

In The Claims:

Claim 1. (currently amended) A chip package structure, comprising:

a substrate, having a lateral surface, a first surface and a second surface, wherein the substrate further has a first metallic layer, a second metallic layer and a conductor with the first metallic layer located on the first surface of the substrate, the second metallic layer located on the second surface of the substrate and the conductor located on the lateral surface of the substrate, and the first metallic layer is electrically connected to the second metallic layer through the conductor, wherein the conductor has a thickness ranging from 0.1 μm to 5 μm ;

a lead frame, located on the first surface of the substrate, wherein the lead frame is electrically connected to the first metallic layer;

a first chip, having a first active surface and a first back surface, wherein the first back surface of the first chip is bonded either onto the surface of the lead frame or onto the first surface, and the first chip has a plurality of first bonding pads on the first active surface;

a plurality of first bonding wires, connecting the first bonding pads of the first chip to the lead frame;

a heat sink, located on the second surface and electrically connected to the second metallic layer; and

a packaging material, encapsulating the first chip, the first bonding wires and a portion of the lead frame, the lead frame having another portion exposed to the ambient.

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Claim 2. (original) The chip package structure of claim 1, wherein the conductor comprises a copper layer.

Claim 3. (cancelled)

Claim 4. (currently amended) The chip package structure of claim 1, wherein the conductor comprises ~~is fabricated using~~ a conductive adhesive.

Claim 5. (cancelled)

Claim 6. (original) The chip package structure of claim 1, further comprising a second chip and a plurality of second bonding wires, wherein the second chip is bonded either onto the lead frame or onto the first surface of the substrate, and the second bonding wires connects the second chip to the lead frame, and the packaging material further encapsulates the second chip and the second bonding wires.

Claim 7. (original) The chip package structure of claim 6, further comprising a plurality of third bonding wires connecting the first chip to the second chip.

Claim 8. (original) The chip package structure of claim 1, wherein the substrate has an insulating layer fabricated using a ceramic material.

Claim 9. (currently amended) A substrate structure with a lateral surface, a first surface and a second surface, comprising:

a first metallic layer, located on the first surface of the substrate;

a second metallic layer, located on the second surface of the substrate; and

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a conductor, located on the lateral surface of the substrate, wherein the first metallic layer is electrically connected to the second metallic layer through the conductor, and the conductor has a thickness ranging from 0.1 μ m to 5 μ m.

Claim 10 (original). The substrate structure of claim 9, wherein the conductor comprises a copper layer.

Claim 11. (cancelled)

Claim 12. (currently amended) The substrate structure of claim 9, wherein the conductor comprises is fabricated using a conductive adhesive.

Claim 13. (cancelled)

Claim 14. (original) The substrate structure of claim 9, wherein the substrate has an insulating layer fabricated using a ceramic material.

Claim 15. (new) The chip package structure of claim 1, wherein the conductor is a composite layer comprising at least two metallic layers.

Claim 16. (new) The chip package structure of claim 15, wherein each of the metallic layers comprises a titanium layer, a titanium-tungsten alloy layer, a copper layer, a nickel layer or a chromium layer.

Claim 17. (new) The substrate structure of claim 9, wherein the conductor is a composite layer comprising at least two metallic layers.

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Claim 18. (new) The substrate structure of claim 18, wherein each of the metallic layers comprises a titanium layer, a titanium-tungsten alloy layer, a copper layer, a nickel layer or a chromium layer.

Claim 19. (new) A method of forming a substrate structure with a lateral surface, a first surface and a second surface, comprising:

forming a first metallic layer on the first surface of the substrate;

forming a second metallic layer, on the second surface of the substrate; and

forming a conductor on the lateral surface of the substrate by using sputtering, evaporation plating, chemical vapor deposition, electroplating or coat-spreading, wherein the first metallic layer is electrically connected to the second metallic layer through the conductor.

Claim 20 (new) The method of claim 19, wherein the conductor has a thickness ranging from 0.1 μm to 5 μm .

Claim 21 (new) The method of claim 19, wherein the conductor is formed comprising:

forming an internal metallic layer on the lateral surface of the substrate; and

forming an external metallic layer over the internal metallic layer.